Stratos II

Preliminary payload electrical specifications

Document version 1.0

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Project Stratos II
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Chapter 1

Flight computer services

As the physical space and mass restrictions for the payloads are strict, the rocket provides the payloads with a number of services. The most important of these are that the rocket supplies the payload with power, data storage and a downlink.

The physical interface with the flight computer consists of a single connector, which must be a Yamaichi NFP-10A-0122BF or equivalent connector. Any equivalent connector must mate with a Yamaichi NFS-10A-0111BF and must have a locking mechanism. The specified connector may be ordered at Farnell, using order code 1143947. The pin-out for the connector is shown in figure 1.1 and table 1.1.

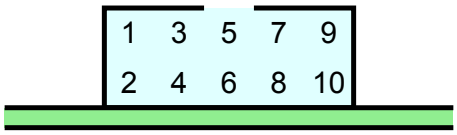

Figure 1.1: Physical pin configuration for the flight computer interface connector, viewed from the side of the payload PCB.

Table 1.1: Pin description for the flight computer interface connector.

Pins	**Symbol**	**Description**
2, 4, 6	0V	Reference voltage.
8, 10	V_{bat}	Supply voltage for the payload, provided by the flight computer.
1	MISO	Data from flight computer to payload.
3	MOSI	Data from payload to flight computer.
5	SCK	Clock for MISO and MOSI, provided by payload.
7	/SS	Slave select signal, provided by payload.
9	V_{bus}	Bus voltage for MISO, MOSI, SCK and /SS, provided by payload.

1.1 Power

As stated, the flight computer provides the payload with some power through the V_{bat} lines. The specifications for the power supply are listed in table 1.2. The maximum supply current per connector is negotiable if multiple slots are reserved for a single payload.

Table 1.2: Payload power specifications.

Symbol	Description	MIN	NOM	MAX	Unit
V_{bat}	Supply voltage for the payload, provided by the flight computer	7.6	10.6	12.6	V
$I_{max,init}$	Maximum switch-on current, $t_{on} < 1$ second			1000	mA
$I_{max,cont}$	Maximum supply current, $t_{on} > 1$ second			100	mA

Warning: the above current specifications are actively policed using current monitors. The power supply to a payload is immediately shut off upon violation of the above rules, to ensure continuity for the other payloads.

1.2 Data

The payload may communicate with the flight computer through a Serial Peripheral Interface (SPI) compliant bus. The bus operates in SPI mode 0 (CPHA = 0, CPOL = 0), see figure 1.2. For convenience for the payload developers, the payload is the master on this bus, such that the payload may determine the SCK frequency depending on their own requirements. The bus voltage is set by the payload as well.

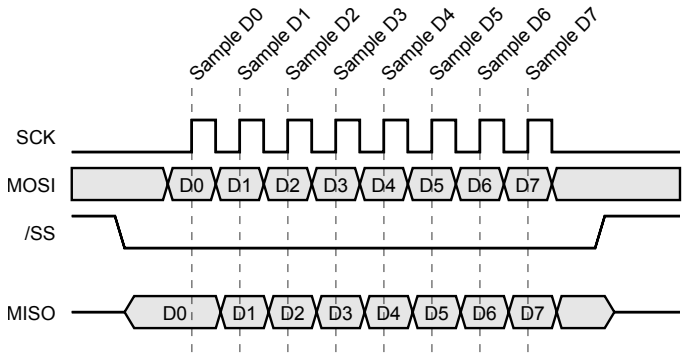

Figure 1.2: Serial Peripheral Interface protocol, mode 0.

1.2.1 Electrical specifications

The bus level translation is handled by four SN74LVC1T45 translators by Texas Instruments, with the payload connected to the A port.

Table 1.3: Data bus electrical specifications.

Symbol	Description	MIN	NOM	MAX	Unit
V_{bus}	Operating bus voltage, provided by the payload.	1.8		5.0	V
$I_{V_{bus}}$	Flight computer current consumption from V_{bus}, $I_{MISO} = 0$			20	μA
V_{IH}	High-level input voltage (MOSI, SCK, /SS)	$V_{bus} \times 0.7$			V
V_{IL}	Low-level input voltage (MOSI, SCK, /SS)			$V_{bus} \times 0.3$	V
I_{OH}	High-level output current (MISO)			-4	mA
I_{OL}	Low-level output current (MISO)			4	mA
V_{OH}	High-level output voltage (MISO), $V_{bus} = 4.5$V	3.8			V
V_{OL}	Low-level output voltage (MISO), $V_{bus} = 4.5$V			0.55	V

1.2.2 Timing specifications

Table 1.4: Data bus timing specifications.

Symbol	Description	MIN	NOM	MAX	Unit
f_{SCK}	SCK clock frequency	0		500	kHz
$t_{SCK,high\ time}$	SCK high time	1.0			μs
$t_{SCK,low\ time}$	SCK high time	1.0			μs
$t_{SS\ to\ SCK}$	SS asserted to first SCK transition	1.0			μs
$t_{SS\ to\ MISO}$	SS released to MISO hi-Z	20.0			ns
$t_{byte\ to\ byte}$	Additional time between two byte transfers	0			μs

1.2.3 Protocol description

The data bus may be used for two purposes:

- Sending data to the flight computer for storage or transmission.
- Reading the flight state of the rocket.

All communications with the flight computer are packet based. The /SS signal is used to delimit the packets. Each packet consists of a command byte and zero or more data bytes. The command byte specifies whether the data provided is to be stored in the flight computer and/or whether it should be transmitted.

Internally, the flight computer has two first-in-first-out (FIFO) buffers, one for the to-be-stored data and one for the to-be-transmitted data. These buffers will be processed by the flight computer as fast as possible, in packets of 8 bytes. This has several implications.

- Data can be transmitted to the flight computer at any rate meeting the timing requirements in table 1.4 until the FIFO buffers are full.
- If the other payloads are not providing data at their maximum allowed rate, the data rate observed by the payload will appear to be higher than specified. It is allowed to exploit this effect, as this does not affect the applied load balancing algorithm.
- If there are less than 8 bytes in the buffer, no data will be processed. To ensure processing of all bytes in a discontinuous data stream, append 8 dummy/pad bytes every time the stream stops for a significant amount of time.

The flight computer will report a 6-bit rocket flight state and the state of the two FIFO buffers in every SPI data transfer. If the FIFO status in the previous transfer indicates that one or both of the selected FIFOs is full, the data sent in the next SPI transfer is ignored.

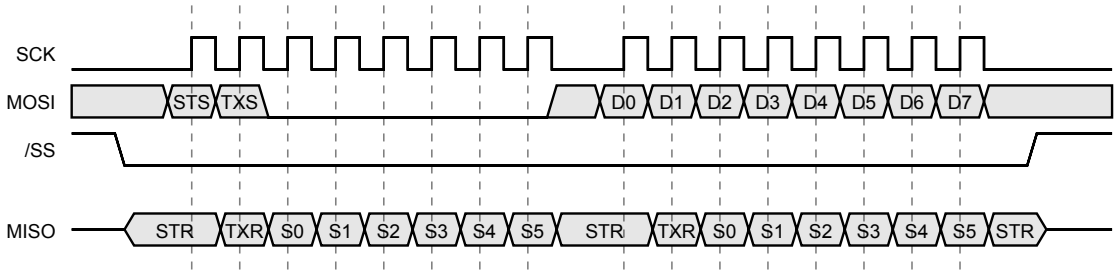

Figure 1.3: Data transfer between payload and flight computer.

Figure 1.3 shows the general case for a data transfer between the payload and the flight computer with one data byte. The symbols used are defined as in table 1.5.

Table 1.5: Description of the symbols used in figure 1.3.

Symbol	**Description**
STS	Storage select. Set to logic high to indicate that the data following the command byte is to be stored in the flight computer storage.
TXS	Transmitter select. Set to logic high to indicate that the data following the command byte is to be transmitted.
STR	Storage FIFO ready. Logic high if the storage FIFO is ready for data.
TXR	Transmitter FIFO ready. Logic high if the transmitter FIFO is ready for data.
D7..0	The data byte, which is either shifted into the selected FIFO buffer(s) or ignored, depending on the values of STS and TXS and the values of STR and TXR in the previous transmission.
S5..0	Rocket flight status. The meaning of the status values is still **TBD** .